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For: UNIVERSALLY ACCESSIBLE FULLY PROGRAMMABLE MEMORY
BUILT-IN SELF-TEST (MBIST) SYSTEM AND METHOD

1 1. A universally accessible fully programmable memory built-in self-test
2 (MBIST) system comprising:
3 an MBIST controller including:
4 an address generator configured to generate addresses for a
5 memory under test;
6 a sequencer circuit configured to deliver test data to selected
7 addresses of said memory under test and reading out that test data;
8 a comparator circuit configured to compare said test data read out
9 of said memory under test to said test data delivered to said memory under test to
10 identify a memory failure, and
11 an externally accessible user programmable pattern register for
12 providing a pattern of test data to said memory under test; and
13 an external pattern programming device configured to supply a said pattern
14 of test data to said user programmable pattern register.

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1 2. The system of claim 1 in which said external programming device includes
2 a computer configured to generate a user defined pattern of test data.

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1 3. The system of claim 1 in which said external programming device includes
2 programmable hardware configured to generate a user defined pattern of test data.

1 4. The system of claim 1 in which said user programmable pattern register
2 includes FLASH memory.

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1 5. The system of claim 1 further including a switch configured to select a
2 computer or programmable hardware to generate a user defined pattern of data.

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1 6. The system of claim 1 in which said user programmable pattern register
2 serially receives said test data from said external pattern programming device.

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1 7. The system of claim 1 in which said user programmable pattern register
2 receives said test data from said external pattern programming device in a parallel
3 configuration.

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1 8. The system of claim 1 in which said user programmable pattern register
2 includes from 1 to N bits.

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1 9. The system of claim 1 in which said user programmable pattern register is
2 located within said MBIST controller.

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1 10. The system of claim 1 in which said user programmable pattern register is
2 located external to said MBIST controller.

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1 11. The system of claim 1 in which said pattern of test data is chosen from the

2 group consisting of: a checkerboard pattern, a diagonal pattern, an all 0's pattern, an all
3 1's pattern, a walking 1's pattern, and a walking 0's pattern, and/or any combination
4 thereof.

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1 12. The system of claim 1 in which said pattern of test data is any defined
2 binary data pattern limited only by the size of said user programmable data register.

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1 13. The system of claim 1 in which said pattern of test data includes any user
2 defined pattern of 1's and 0's.

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1 14. The system of claim 1 further including a multiplexor where a test mode
2 signal selects said addresses generated from said address generator or system addresses
3 based on a predetermined state of said test mode signal.

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1 15. The system of claim 1 further including a multiplexor where a test mode
2 signal selects said pattern of test data or system data based on a predetermined state of
3 said test mode signal.

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1 16. A universally accessible fully programmable memory built-in self-test
2 (MBIST) system, the system comprising:
3 an MBIST controller including:
4 an address generator configured to generate addresses for a
5 memory under test;
6 a sequencer circuit configured to deliver test data to selected
7 addresses of said memory under test and reading out that test data, and
8 a comparator circuit configured to compare said test data read out
9 of said memory under test to said test data delivered to said memory under test to
10 identify a memory failure;
11 an externally accessible user programmable pattern register remote from
12 said MBIST controller for providing a pattern of test data to said memory under test; and
13 an external pattern programming device configured to supply said pattern
14 of test data for said user programmable data pattern register.

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1 17. A universally accessible fully programmable memory built-in self-test
2 (MBIST) method, the method comprising:
3 generating addresses for a memory under test;
4 generating for an externally accessible user programmable pattern
5 register a pattern of test data with an external pattern programming device;
6 programming said user programmable pattern register with said
7 pattern of test data to said memory under test;
8 delivering test data to selected addresses of said memory under
9 test;
10 reading out said test data from said selected addresses of said
11 memory under test; and
12 comparing said test data read out of said memory under test to said
13 test data delivered to said memory under test to identify a memory failure.